WHAT IS CLAIMED IS:

1.

A memory array comprising:

a first set of nanoscale wires;

a second set of nanoscale wires intersecting the first set of nanoscale wires, intersections between the first set and the second set defining memory locations;

wherein the memory locations are addressed by selecting one nanoscale wire of the first set of nanoscale wires and one wire of the second set of nanoscale wires;

wherein nanoscale wires of the first set and nanoscale wires of the second set comprise controllable regions axially distributed along the nanoscale wires, a first set of the controllable regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property;

the memory array further comprising:

a first plurality of addressing wires, each addressing wire of the first plurality associated with a series of regions of the first set of nanoscale wires; and

a second plurality of addressing wires, each addressing wire of the second plurality associated with a series of regions of the second set of nanoscale wires.

2.

The memory array of claim 1, wherein the first set of controllable regions allow conduction along the nanoscale wire when each region of the first set is either controlled with a signal having a value lower that a first threshold or is not controlled.

3.

The memory array of claim 1, wherein the first set of controllable regions allow conduction along the nanoscale wire when each region of the first set is controlled with a signal having a value higher than a first threshold.

4.

The memory array of claim 1, wherein the difference between the first physical property and the second physical property is based on different doping levels of the controllable regions.

5.

The memory array of claim 1, wherein the difference between the first physical property and the second physical property is based on different materials of the controllable regions.

6.

The memory array of claim 1, wherein the addressing wires allow a memory location to be into one of a plurality of states.

7.

The memory array of claim 1, wherein the addressing wires allow a state of a memory location to be read.

8.

The memory array of claim 1, wherein the memory locations are addressed in a reading operation.

9.

The memory array of claim 1, wherein the memory locations are addressed in a writing operation.

10.

The memory array of claim 1, further comprising microscale wires acting as ohmic contacts.

11.

The memory array of claim 1, further comprising microscale wires allowing signals to be disconnected from the nanoscale wires.

12.

The memory array of claim 1, wherein the microscale wires control FET-controllable regions.

13.

The memory array of claim 1, wherein the memory locations are defined by means of programmable diode-type crossbar junctions between the first set and the second set.

14.

The memory array of claim 1, wherein the memory locations are defined by means of FET-type crossbar junctions between the first set and the second set.

15.

The memory array of claim 1, wherein nanoscale wires of one set among the first set and a second set of nanoscale wires comprise controllable doped regions radially distributed along the nanoscale wires, the radially distributed controllable doped regions allowing information to be stored at the memory locations.

16.

The memory array of claim 1, wherein the regions of the first and second set are made of different materials.

17.

The memory array of claim 1, wherein the addressing wires are microscale wires.

18.

The memory array of claim 1, wherein the addressing wires are nanoscale wires.

19.

The memory array of claim 1, wherein the first set of nanoscale wires is part of a larger set of nanoscale wires, the first set being selected from the larger set by means of a microscale wire acting as an ohmic contact.

20.

The memory array of claim 1, wherein the first and second set of nanoscale wires are part of larger sets of nanoscale wires, the first and second set being selected from the larger sets by means of microscale wires acting as ohmic contacts.

21.

A circuit for selecting a nanoscale wire among a plurality of nanoscale wires, comprising:

microscale ohmic contacts, each ohmic contact connected to a different subset of the plurality of nanoscale wires for selecting a specific subset of the plurality of nanoscale wires; and

addressing wires associated with the different subsets of the plurality of nanoscale wires, for selecting a nanoscale wire among the specific subset of nanoscale wires once the specific subset has been selected.

22.

The circuit of claim 21, wherein the addressing wires are microscale wires.

23.

The circuit of claim 21, wherein the addressing wires are nanoscale wires.

24.

The circuit of claim 21, wherein the microscale ohmic contacts are designed to abut tightly to leave not more than a sublithographic sized gap of unaddressable nanowires between them.

25.

The circuit of claim 21 or 24, wherein the microscale ohmic contacts are staggered there-between.

26.

A memory array comprising:

a plurality of nanoscale wires;

a first set of microscale wires intersecting the nanoscale wires, intersections between the first set of microscale wires and the nanoscale wires defining address locations to address one or more nanoscale wires among the plurality of nanoscale wires; and

a second set of microscale wires intersecting the nanoscale wires, intersections between the second set of microscale wires and the nanoscale wires defining memory locations.

27.

The memory array of claim 26, wherein the memory locations are selected by selecting one nanoscale wire and one microscale wire of the second set of microscale wires.

28.

The memory array of claim 26, wherein the nanoscale wires comprise controllable regions axially distributed along the nanoscale wires, a first set of the controllable regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property.

29.

The memory array of claim 28, wherein the difference between the first physical property and the second physical property is based on different doping levels of the controllable regions.

30.

The memory array of claim 28, wherein the difference between the first physical property and the second physical property is based on different materials of the controllable regions.

31.

The memory array of claim 28, wherein the first set of controllable regions allow conduction along the nanoscale wire when each region of the first set is either controlled with a signal having a value lower than a first threshold or is not controlled.

32.

The memory array of claim 28, wherein the first set of controllable regions allow conduction along the nanoscale wire when each region of the first set is controlled with a signal having a value higher than a first threshold.

33.

The memory array of claim 26, wherein the memory locations are addressed in a reading operation.

34.

The memory array of claim 26, wherein the memory locations are addressed in a writing operation.

35.

The memory array of claim 26, further comprising microscale ohmic contacts, each ohmic contact connected to a different subset of the plurality of nanoscale wires for selecting a specific subset of the plurality of nanoscale wires.

36.

The memory array of claim 35, wherein the microscale ohmic contacts are staggered there-between.

37.

A three-dimensional memory array comprising:

a plurality of layers of nanoscale wires, intersections between nanoscale wires of a first layer and nanoscale wires of a second layer adjacent to the first layer defining memory locations;

a plurality of microscale contacts connected to nanoscale wires of different layers of nanoscale wires;

wherein the nanoscale wires comprise controllable regions axially distributed along the nanoscale wires, to allow addressing of the nanoscale wires, a first set of the controllable regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property.

38.

The three-dimensional memory array of claim 37, wherein the layers of nanoscale wires are so arranged to define repeated occurrences of adjacent sets of layers comprising:

a first layer of memory-location-defining nanoscale wires;

a second layer of memory-location-defining nanoscale wires; and

a layer of insulating nanoscale wires.

39.

The three-dimensional memory array of claim 37, wherein nanoscale wires located on different layers and sharing a microscale contact are each independently addressable.

40.

The three-dimensional memory array of claim 37, wherein groups of the nanoscale wires can be independently addressed, the number of groups being a large fraction of the number of nanowires in the array.

41.

A process for manufacturing a logic arrangement having microscale and nanoscale wires, comprising:

providing microscale wires;

determining an addressing portion on the microscale wires;

transferring a first set of aligned nanoscale wires over the microscale wires; and

transferring a second set of aligned nanoscale wires over the microscale wires and the first set of nanoscale wires, orthogonally to the first set of nanoscale wires.

42.

The process of claim 41, wherein alignment of the first set and second set of the nanoscale wires is obtained by means of a LB-flow technique.

43.

The process of claim 41, further comprising axially doping the nanoscale wires.

44.

The process of claim 41, further comprising radially doping the nanoscale wires.

45.

The process of claim 41, further comprising axially and radially doping the nanoscale wires.

46.

The process of claim 45, further comprising etching away a radially doped portion from the nanoscale wires.

47.

The process of claim 41, further comprising etching breaks in the nanowires.